HARDWARE/SOFTWARE CO-VERIFICATION METHOD

ABSTRACT OF THE DISCLOSURE

A hardware/software co-verification method that achieves fast simulation execution by implementing a C-based native code simulation without degrading the accuracy of timing verification. This method is a method for co-verifying hardware and software, by using a host CPU, for a semiconductor device on which at least one target CPU and one OS are mounted wherein, first, a timed software component described in a C-based language or constructed from binary code native to the host CPU and a hardware component described in the C-based language are input as verification models, necessary compiling is performed, and the compiled components are linked together. Next, a testbench is input and compiled. Then, the components and the testbench are linked together, after which simulation is performed and the result of the simulation is output.